AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0026] with the following amended paragraph:

FIGURE 13 is a cross sectional view of a semiconductor wafer illustrating the thirteenth t~~h~~embodiment according to the present invention.

Please replace paragraph [0038] with the following amended paragraph:

The present invention proposes a novel structure for charge trapping nonvolatile memory. In the structure, the cell capacity for storing data can be increased by the cell structure. The detail description will be seen as follows. A semiconductor substrate is provided for the present invention. In a preferred embodiment, as shown in the FIGURE 1, a single crystal silicon substrate 2 with a <100> or <111> crystallographic orientation is provided. The substrate 2 includes a pattern of active areas. The isolation to separate the devices includes STI or FOX. A thin dielectric layer 4 consisted of silicon dioxide is formed on the substrate 2 to act as gate oxide. Typically, the layer 4 can be grown in oxygen ambient at a temperature of about 700 to 1100 degrees centigrade. Other method, such as chemical vapor deposition, can also form the oxide. In the embodiment, the thickness of the silicon dioxide layer 4 is approximately 15-250 angstroms. Subsequently, a conductive layer 6 is formed on the layer 4. The conductive layer 4~~6~~ may be formed of doped polysilicon, in-situ doped polysilicon or epitaxy silicon. For an embodiment, the doped polysilicon layer 6 is doped by phosphorus using a PH_3 source. A photo-resist defined patterning process is used on the conductive layer 6, thereby forming the gate structure on the silicon substrate 2. It has to be noted that the gate structure includes a charge trapping region 8 located at lower portion of the spacer 12 adjacent to the gate 6. Please refer to FIGURE 1, an isolation layer 10 is conformally formed on the substrate 2 and the gate structure 6. The material for forming the isolation layer 10 can be oxide (SiO_2) or (HfO_2) or the material with energy gap higher than 7 eV. One suitable method for the oxide layer 10 includes thermal oxidation and deposition by CVD. For example, Low Pressure Chemical Vapor Deposition (LPCVD), Plasma Enhance Chemical Vapor Deposition (PECVD), High Density Plasma Chemical Vapor Deposition (HDPCVD). Still

referring to FIGURE 1, an isotropic etching is performed to create sidewall spacers 12 on the sidewall of the isolation layer 10. Reactive ion etching (RIE) or plasma etching is the typical way to achieve the purpose. The spacers 12 includes the charge trapping region 8, thereby forming the ON structure capable of trapping carriers to define the digital states. The material for the spacer could be nitride or the material with energy gap smaller than 6 eV. In the preferred embodiment, the reaction gases of the step to form silicon nitride layer include, for example, SiH4, NH3N2, N2O or SiH2Cl2, NH3N2,N2O

Please replace paragraph [0039] with the following amended paragraph:

Turning to FIGURE 1, the p-n junction of source and drain region 14 is formed by performing an ion implantation to dope ions into the substrate 2 using the gate structure 6 and sidewall spacers 12 as a mask. After selectively etching isolation layer 10, portions of the gate 6 and substrate 2 are exposed. Silicide 16 is introduced on the exposed surface of the top portion of gate and the silicon substrate 2 on the source and drain regions 14 to reduce their resistance. Preferably, the silicide 16 can be $TiSi_2$, WSi_2, $CoSi_2$ or NiSi. The gate structure 6 acts as the control gate, and the nitride spacers are used to trap carriers. The spacers 12 are used to store charges, thereby defining the digital states including (0, 0), (0, 1), (1, 0), (1, 1). A sectional view of a multi-bit nonvolatile memory cell in accordance with the present invention is shown in FIG. 1-24. The memory cell includes a substrate 2 having at least two buried PN junctions, one is the left junction and the other is the right junction. Channels are located between the two junctions during operation. Above the main channel is an oxide 4, on top of the oxide layer 4 is a control gate 6. Spacer 12 is used for charge trapping and is preferably comprised of silicon nitride. The hot electrons or holes are trapped as they are injected into the Spacer 12. The stack structure including the spacer 12 and the isolation layer 10 refers to the spacer trapping structure, as shown in figure 1.

Please replace paragraph [0042] with the following amended paragraph:

Turning to figure 3, the embodiment includes pocket ion implantation region 18 adjacent to the source and drain region 14 and adjacent to the gate structure to reduce the short channel effect and increase the efficiency of the hot carrier injection. Figure 4 shows the ~~alterative~~alternative example for the present invention, it is similar to the second embodiment. It also includes pocket ion implantation region 18 adjacent to the source and drain region 14. The conductive type of the pocket implant region 18 is opposite to the one of the source and drain region 14.

Please replace paragraph [0043] with the following amended paragraph:

Figures 5 and 6 are the alternative approaches with respect to the embodiments shown in figures 3 and 4. The fifth and sixth embodiments introduce the lightly doped drain 14a to control the hot carriers and further comprise pocket ion implant region 18 adjacent to the source and drain region 14 and under the portion 8 of the charge trapping spacers 12. The conductive type of the pocket ion implantation region is opposite to the one of the source and drain region. The junction of the lightly doped drain is shallower than the one of the source and drain region. The lightly doped drain 14b is also closer to the channel under the gate. Alternatively, the other embodiments shown in figures 7 and 8 introduce the usage of double diffused drain (DDD) structure to reduce the junction breakdown effect. The conductive ion type of the DDD structure is the same as that of the source and drain region. However, the junctions of the lightly doped regions are deeper than the junctions of the heavily doped source and drain region. The embodiments further comprise pocket ion implant region adjacent to the double diffused source and drain region and under the spacer structure 8 of the control gate 6.